

### PROGRAM 20 NOVEMBER ROOM

<b>08:00-08:30</b>	Registration.	
<b>08:30-09:00</b>	Opening.	
<b>09:00-10:00</b>	<b>KEYNOTE SESSION.</b> José M. de la Rosa. _____ <i>Efficient Digitizers for a Digital-Driven World.</i>	<b>BAROJA</b>
<b>10:00-10:30</b>	Coffee Break.	
<b>10:30-12:30</b>	<b>1A TEST, RELIABILITY AND MODELING</b> _____	<b>BAROJA</b>
	<b>1B VARIABILITY-AWARE DESIGN AND TOOLS</b> _____	<b>ARRIAGA</b>
<b>12:30-14:00</b>	Lunch break.	
<b>14:00-16:00</b>	<b>2A ULTRA-LOW POWER SYSTEMS</b> _____	<b>BAROJA</b>
	<b>2B SPECIAL SESSION: SMART FARMING I</b> _____	<b>ARRIAGA</b>
<b>16:00-16:30</b>	Coffee Break. Poster Presentation: participants explain their contribution. _____	<b>LABOA</b>
<b>16:30-18:30</b>	<b>3A FPGA DESIGN</b> _____	<b>BAROJA</b>
	<b>3B SPECIAL SESSION: SMART FARMING II</b> _____	<b>ARRIAGA</b>
<b>19:00-21:00</b>	"Old Town of Bilbao" guided tour & Pintxo Pote (depart from the venue).	

### PROGRAM 21 NOVEMBER

<b>08:00-09:00</b>	Registration.	
<b>09:00-10:00</b>	<b>KEYNOTE SESSION.</b> Carmen G. Almudéver. _____ <i>Full-stack challenges of bridging quantum chips up to scalable quantum co-processor heterogeneous architectures: The art of multidisciplinary science.</i>	<b>BAROJA</b>
<b>10:00-10:30</b>	Coffee Break. Poster Presentation: participants explain their contribution. _____	<b>LABOA</b>
<b>10:30-12:30</b>	<b>4A SYSTEM-ON-CHIPS AND HIGH PERFORMANCE DESIGN</b> _____	<b>BAROJA</b>
	<b>4B EMERGING TECHNOLOGIES FOR CIRCUITS AND SYSTEMS</b> _____	<b>ARRIAGA</b>
<b>12:30-14:00</b>	Lunch break.	
<b>14:00-16:00</b>	<b>5A POWER ELECTRONICS</b> _____	<b>BAROJA</b>
	<b>5B INDUSTRIAL AND MEDICAL APPLICATIONS</b> _____	<b>ARRIAGA</b>
<b>15:45-16:30</b>	<i>2019 meeting of IEEE CAS Spain Chapter.</i> _____	<b>BARANDIARAN</b>
<b>16:00-16:30</b>	Coffee break.	
<b>16:30-18:30</b>	<b>PANEL: Women and Engineering. Best paper award of IEEE CEDA Spain.</b> _____	<b>BAROJA</b>
<b>20:00-24:00</b>	Conference Dinner at Yandiola - Azkuna Zentroa.	

### PROGRAM 22 NOVEMBER

<b>09:30-10:30</b>	<i>Advanced methods for integrated circuits and high speed digital interface validation.</i> _____	<b>BAROJA</b>
<b>09:30-10:30</b>	<i>2019 meeting of IEEE CEDA Spain Chapter</i> _____	<b>BARANDIARAN</b>
<b>10:30-11:30</b>	<b>KEYNOTE SESSION.</b> Nicola Delmonte. _____ <i>Cooling techniques for power electronics: 3D and compact modeling for accurate thermal simulations.</i>	<b>BAROJA</b>
<b>11:30-12:30</b>	Best PhD poster award in DCIS 2019. Closing Ceremony. _____	<b>BAROJA</b>
<b>12:30-14:00</b>	Lunch.	