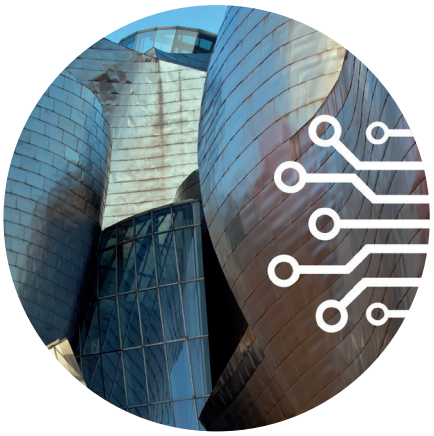

DCIS 2019

XXXIV Conference on Design of Circuits and Integrated Systems

20-22 November. Bilbao (Spain)

Organizer

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08:00-08:30 Registration.

08:30-09:00 Opening.

09:00-10:00 **KEYNOTE SESSION.** ***Efficient Digitizers for a Digital-Driven World.*** **BAROJA ROOM**

Co-sponsored by the Spain Chapter of IEEE CAS.

José M. de la Rosa. Vicedirector of the Institute of Microelectronics of Seville (IMSE) and Full Professor at the Dept. of Electronics and Electromagnetism of the University of Seville (Spain).

Data converters are key enablers for the feasible implementation of coming cyber-physical devices connected in the Internet-of-Things (IoT), where the analog/digital (A/D) interface constitutes one of their main design bottlenecks. Year after year, a number of circuits and systems techniques are embedded in different architectures of Analog-to-Digital Converters (ADCs) in order to cover a wider resolution-vs-speed conversion range. The limits of energy efficiency of ADCs are continuously pushed in order to digitize very diverse types of signals in many different applications – from ultra-low-power biomedical devices to ultra-wide-band communications.

This lecture gives an overview of some emerging data-conversion strategies at the forefront of the state of the art, which will enable the implementation of new technology paradigms such as the so-called software-defined electronics and cognitive radio. A number of trends and design challenges in the design of efficient digitizers will be discussed, as well as the implications derived from their integration in deep-nanometer CMOS. Main limitations and problems faced by cutting-edge designs as well as tendencies, research opportunities and perspectives on the evolution of data converters will be envisioned, highlighting how they can improve their performance and efficiency in an increasingly digital-driven world.

10:00-10:30 Coffee Break.

10:30-12:30 **1A TEST, RELIABILITY AND MODELING** **BAROJA ROOM**

Chairman: **Mikel Roca.** University of the Balearic Islands.

10:30 ***Fast Simulation of Non-linear Circuits using Semi-Analytical Solutions based on the Matrix Exponential.***
Juan Alfonso Serrano, Antonio José Ginés, Eduardo Peralias, Adoración Rueda.

10:55 ***Applying Model Checking in the Verification of a Clock Masking Unit.***
José Leitão, Marcelino Santos.

11:20 ***On the Use of Built-in Temperature Sensors to Monitor Aging in RF Circuits.***
Anant Rungta, Josep Altet, Enrique Barajas, Xavier Aragonés, Diego Mateo.

11:45 ***Reliability and Accelerated Testing of 14nm FinFET Ring Oscillators.***
Shu-han Hsu, Kexin Yang, Linda Milor.

12:10 ***An Alternative SNR Computation Method for ADC Testing.***
José Machado da Silva, José Carlos Alves.

10:30-12:30 **1B VARIABILITY-AWARE DESIGN AND TOOLS** **ARRIAGA ROOM**

Chairman: **Antonio Rubio.** Polytechnic University of Catalonia.

10:30 ***Weak and Strong SRAM cells analysis in embedded memories for PUF applications.***
Abdel ALheyasat, Gabriel Torrens, Sebastià Bota, Bartomeu Alorda.

10:55 ***Assessing SET Sensitivity of Mixed-Signal Circuits at Early Design Stages.***
Aránzazu Fernández-Álvarez, Marta Portela-García, Mario García-Valderas, Celia López-Ongil, Servando Espejo.

10:30-12:30 **1B VARIABILITY-AWARE DESIGN AND TOOLS** **ARRIAGA ROOM**

11:20 ***SET sensitivity evaluation, a comparison before and after layout.***
Valentín Gutiérrez.

11:45 ***Test Vehicle Design for Single-Event Transient Analysis of Switched-Capacitor Circuits.***
Jorge Jiménez-Sénchez, Jose María Hinojo, Fernando Márquez, Rogelio Palomo, Manuel Pedro Carrasco, Fernando Muñoz.

12:10 ***Mismatch and Offset Calibration in Redundant SAR ADC.***
Antonio López-Angulo, Antonio Gines, Eduardo Peralias, Adoración Rueda.

12:30-14:00 Lunch break.

14:00-16:00 **2A ULTRA-LOW POWER SYSTEMS** **BAROJA ROOM**

Chairwoman: **Mar Martínez.** University of Cantabria.

14:00 ***A 365mV, 13nW CMOS-only energy harvested reference voltage for RFID applications in 40nm technology.***
Asghar Bahramali, Marisa López-Vallejo, Carlos López Barrio.

14:25 ***A 28 uW timing circuit for a 60 um2 HV-CMOS pixel.***
Sergio Moreno, Óscar Alonso, Ángel Diéguez, Eva Vilella, Gianluigi Casse, Joost Vossebeld.

14:50 ***Design of ULV ULP LNAs Exploiting FBB in FDSOI 28nm Technology.***
Xavier Aragones, Álex Álvarez, Juan Pablo Rovayo, Josep Altet, Diego Mateo.

15:15 ***Review of Bandgap Voltage Reference Architectures for Long-Range Passive RFID Applications.***
Josu Catalina.

2B SPECIAL SESSION: SMART FARMING I **ARRIAGA ROOM**

Chairman: **Luis Entrena.** Carlos III University.

14:00 ***A spectral imaging system for precision agriculture: from its inception till a pre-commercial prototype.***
Pablo Horstrand.

14:25 ***The PLATINO Experience: A LoRa-based Network of Energy-Harvesting Devices for Smart Farming.***
Soledad Escolar, Xavier del Toro, Félix J. Villanueva, Maria J. Santofimia, David Villa, Jesús Barba, Fernando Rincón, Juan Carlos López.

14:50 ***Aerial-Ground collaborative pathfinding using HLSTL (HLS library for generic IP development on FPGAs).***
Manuel J. Abaldea, Jesús Barba, Julián Caba, Fernando Rincón, Juan Carlos López.

15:15 ***Characterizing Hyperspectral Data Layouts: Performance and Energy Efficiency in Embedded GPUs for PCA-based Dimensionality Reduction.***
Jaime Sancho Aragón, Sergio Sánchez Ramírez, Raquel Lazcano López, Daniel Madroñal Quintín, Rubén Salvador Perea, Eduardo Juárez Martínez, César Sanz Álvaro.

15:40 ***Real-time hyperspectral image compression: a low consumption approach for UAV-based applications.***
María Díaz, Raúl Guerra, Pablo Horstrand, Ernestina Martel, Sebastián López, José F. López, Roberto Sarmiento.

16:00-16:30 Coffee Break. **LABOA ROOM**
Poster Presentation: participants explain their contribution.

16:30-18:30 3A FPGA DESIGN — BAROJA ROOM

Chairman: **Jesus Lázaro.** UPV/EHU.

16:30 ***Implementation feasibility of a lossless data compression IP core compliant with the CCSDS 121.0-B-2 standard on space-qualified FPGAs.***
Yubal Barrios, Antonio Sánchez, Lucana Santos, Roberto Sarmiento.

16:55 ***SHyLoC 2.0 CCSDS-123 IP: improving CCSDS 123.0-B-1 standard compliant IP core for on-board lossless compression of hyperspectral images.***
Antonio José Sánchez, Yubal Barrios, Lucana Santos, Roberto Sarmiento.

17:20 ***HLS code refactoring using SDSoC applied to multiclass SVM classification of Hyperspectral Images.***
Abelardo Báez Quevedo, Himar Fabelo Gómez, Samuel Ortega Sarmiento, Gustavo Marrero Callicó, Roberto Sarmiento Rodríguez.

17:45 ***Time-Domain Coding for Resource-Efficient Deep Neural Networks.***
Sergio Avalos-Legaz, Pablo Ituero.

18:10 ***Hardware Implementation of Statecharts for FPGA-based Control in Scientific Facilities.***
Roberto Rodríguez Osorio, Javier Cereijo-García.

3B SPECIAL SESSION: SMART FARMING II — ARRIAGA ROOM

Chairman: **Roc Berenguer.** University of Navarre.

16:30 ***Design Space Exploration on Heterogeneous Platforms Using OpenMP.***
Ángel Álvarez, Íñigo Ugarte, Víctor Fernández, Pablo Sanchez.

16:55 ***Optimal UAV movement control for farming areas scanning using hyperspectral pushbroom sensors.***
Raúl Guerra, Pablo Horstrand, María Díaz, Sebastián López, José F. López.

17:20 ***Hardware Accelerator for Ethanol Detection in Water Media based on Machine Learning Techniques.***
Rodrigo Marino, Sergio Quintero, Jose M. Lanza-Gutiérrez, Teresa Riesgo, Miguel Holgado, Jorge Portilla, Eduardo de la Torre.

17:45 ***Artificial Vision on Edge IoT Devices: A Practical Case for 3D Data Classification.***
Cristian Wisultschew, José Andrés Otero, Jorge Portilla.

18:10 ***Low-Cost Hyperspectral Push-broom Microscope, targeting Smart Farming Applications.***
Samuel Ortega, Raúl Guerra, Himar Fabelo, María Díaz, Sebastián López, Gustavo M. Callicó, Roberto Sarmiento.

19:00-21:00 "Old Town of Bilbao" guided tour & Pintxo Pote (depart from the venue).

08:00-09:00 Registration.

09:00-10:00 **KEYNOTE SESSION.** ***Full-stack challenges of bridging quantum chips up to scalable quantum co-processor heterogeneous architectures: The art of multidisciplinary science.*** **BAROJA ROOM**

Carmen G. Almudéver. Quantum Computer Architecture Lab, QuTech, Delft University of Technology, The Netherlands.

Quantum computers promise to solve a certain set of hard problems that are intractable for even the most powerful current supercomputers. Remarkable progress has been made in recent years in quantum hardware, and quantum computation in the cloud is already a reality offering small quantum processors that are capable of handling basic quantum algorithms. Main IT companies like Google, Intel, Microsoft and IBM and numerous research groups are working on building the first universal quantum computer. Building such a quantum system requires bridging quantum algorithms and quantum processors. This talk will address first the state of the art in quantum computing, emphasizing the main challenges that include improvement and scalability of quantum processors, classical control electronics at (possibly) cryogenic temperatures and definition of a heterogeneous quantum computer architecture. Then, a discussion on the system architecture focusing on making quantum computing fault-tolerant and the compilation of quantum circuits will be presented. In the last part of the talk, I will provide my vision on how the research community could accelerate the process towards building such a scalable quantum machine, potentially through vertical cross-layer co-design structured methodologies, and possible applications, particularly quantum-enhanced Deep Learning co-processors.

10:00-10:30 Coffee Break. **LABOA ROOM**
Poster Presentation: participants explain their contribution.

10:30-12:30 **4A SYSTEM-ON-CHIPS AND HIGH PERFORMANCE DESIGN** **BAROJA ROOM**

Chairman: **Antonio López Martín.** Public University of Navarre.

10:30 ***Deep Packet Inspection through Virtual Platforms using System-on-Chip FPGAs.***
Raquel León, Adrián Domínguez, Pedro P. Carballo, Antonio Núñez.

10:55 ***An interconnect-Centric Approach to the Flexible Partitioning and Isolation of Many-core Accelerators for Fog Computing.***
Davide Bertozzi, Meriem Turki.

11:20 ***Efficient Elliptic Curve Cryptoprocessor for enabling TLS protocol in low-cost reconfigurable SoCs.***
Luis Parrilla, Ahmed Mohamed Bellemou, Antonio García, Encarnación Castillo.

11:45 ***Self-Organizing Maps hybrid Implementation Based on Stochastic Computing.***
Alejandro Morán-Costoya, Josep L. Rosselló, Miquel Roca, Eugeni Isern, Victor Martínez-Moll, Vincent Canals.

12:10 ***Accelerating the Binaural Sound Synthesis on low-power ARMv7 Multicore Processors.***
Jose A. Belloch, José M. Badía, Almudena Lindoso, Germán León, Luis Entrena.

4B EMERGING TECHNOLOGIES FOR CIRCUITS AND SYSTEMS **ARRIAGA ROOM**

Chairwoman: **Linda Milor.** Georgia Institute of Technology.

10:30 ***Assessing the Effectiveness of the Test of Power Devices at the Board Level.***
Davide Piumatti, Stefano Borlo, Fabio Mandrile, Matteo Sonza Reorda, Radu Bojoi.

10:55 ***3D Printed 5-Order Butterworth Passive Filter with Conical Inductors for RF Broadband Applications.***
Arnau Salas Barenys, Neus Vidal Martínez, Josep Maria López.

11:20 ***Device circuit co-design of HyperFET transistors.***
Manuel Jiménez, Juan Núñez, María J. Avedillo.

11:45 ***Design considerations and architectures for 250 GHz LNAs in SiGe technology.***
Urko Nieto, David del Rio, Iñaki Gurutzeaga, Héctor Solar, Roc Berenguer.

12:10 ***Design of integrated control circuits for mm-wave phased arrays in 55-nm BiCMOS.***
David del Río, Andoni Irizar, Iñaki Gurutzeaga, Ainhoa Rezola, Roc Berenguer, Juan Francisco Sevillano.

12:30-14:00 Lunch break.

14:00-16:00 **5A POWER ELECTRONICS** — **BAROJA ROOM**

Chairman: **Nicola Delmonte.** University of Parma.

14:00 ***Super Class AB OTA Based on Current-Starved Nonlinear Mirrors and Dynamic Biasing.***
Antonio López-Martin, Jose M. Algueta, M. Pilar Garde, Ramon G. Carvajal, Jaime Ramírez-Angulo.

14:25 ***A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications.***
David Galante Sempere, Daniel Mayor Duarte, Mario San Miguel Montesdeoca, Sunil Lalchand Khemchandani, Javier del Pino.

14:50 ***Power Amplifiers Load Modulation Techniques for 5G in GaN-on-Si Techonology.***
Victoria Díez Acereda, Ayoze Diaz Carballo, Roberto Rodríguez Hernández, Javier del Pino, Sunil Lalchand Khemchandani.

15:15 ***FPGA and CPU based real-time simulation platform for EV propulsion system analysis under driving cycles.***
Markel Fernández, Edorta Ibarra, Endika Robles, Oihane Cuñado, Maite Aranguren, Iñigo Kortabarria, Yahia Bouzid.

15:40 ***Fast and efficient prototype system for embedded control algorithms in electric traction.***
Carlos Cuadrado Viana.

5B INDUSTRIAL AND MEDICAL APPLICATIONS — **ARRIAGA ROOM**

Chairman: **José Machado da Silva.** University of Porto.

14:00 ***Accelerating Host-Compiled Simulation by Modifying IR code: Industrial application in the spatial domain.***
Hector Posadas, Eugenio Villar.

14:25 ***A plethysmographic sensor for monitoring volumen changes in cardiovascular pathologies.***
Enrique Rando, Gloria Huertas, Alberto Yufera.

14:50 ***Resolution enhancement of VCO-based ADCs by passive interpolation and phase injection.***
Leidy Mabel Alvero González, Eric Gutiérrez Fernandez, Luis Hernández Corporales.

15:15 ***Dermatologic Hyperspectral Imaging System for Skin Cancer Diagnosis Assistance.***
Himar Fabelo, Verónica Melian, Beatriz Martínez, Patricia Beltrán, Samuel Ortega, Margarita Marrero, Gustavo M. Callicó, Roberto Sarmiento.

15:45-16:30 ***2019 meeting of IEEE CAS Spain Chapter.*** — **BARANDIARAN ROOM**

16:00-16:30 Coffee break.

16:30-18:30 ***Best paper award of the IEEE CEDA Spain Chapter.*** — **BAROJA ROOM**

PANEL: Women and Engineering.
"Where are we? Where should we be? How to get there?"

Co-sponsored by the Spain Chapter of IEEE CEDA.
Organizers: Francisco Fernández (CEDA, Univ. Sevilla), Carlos López Barrio (UPM), Marisa López Vallejo (UPM).
Participants: Teresa Riesgo (UPM and Dirección General de Investigación, Desarrollo e Innovación Spanish Government), Celia López Ongil (Univ. Carlos III), Julia Merino Fernández (Tecnalia), Linda Milor (Georgia Tech), Eduard Alarcon (UPC).

How to promote STEM degrees between female students.
Women in male-dominated professions. Is it a problem?
Promotion of women to leadership positions. Which are the obstacles?
Is society taking the correct measures? Is our community taking the correct measures? Should we take measures?".

20:00-24:00 Conference Dinner at Yandiola - Azkuna Zentroa.

09:30-10:30 ***Advanced methods for integrated circuits and high speed digital interface validation.*** **BAROJA ROOM**

Victor Medina. Rohde & Schwarz.

In this session some improvements and news in state of the art techniques for circuit design tests are presented, such as eye diagram with real time deembedding and TDR/TDT analysis. In parallel, the new high performance oscilloscope R&S RTP is introduced.

09:30-10:30 ***2019 meeting of IEEE CEDA Spain Chapter*** **BARANDIARAN ROOM**

10:30-11:30 **KEYNOTE SESSION.** ***Cooling techniques for power electronics: 3D and compact modeling for accurate thermal simulations.*** **BAROJA ROOM**

Nicola Delmonte. Research Fellow, Assistant Professor and Associate Professor of the Department of Engineering and Architecture of the University of Parma (Italy).

Thermal management is a key point of power converters design because it limits their performance determining heat flows, as well as reliability. Even if cooling technologies for electronics have been a research topic since the birth of power electronics, in the last decade the number of publications related to this field has grown significantly. This is because thermal management, with the power density increasing and the high reliability required by many applications, cannot be the same of old systems.
Then, here it will be presented the state of the art of cooling techniques for power electronics and the numerical modeling related to thermal management problems.
Starting from standard techniques based on natural and forced convective systems, both with air and liquids, others high efficiency cooling systems, such as those based on electrowetting, immersion, and phase change coolants, will be shown. Together with cooling techniques, some standard and innovative technologies to produce power modules, designed to improve both electrical and thermal performances, will be presented. It will be shown how to model these systems for multiphysics Finite Element Analysis, considering the heat transfer coupled to electromagnetic or fluid dynamics physics.
Finally, it will be shown a different kind of numerical analysis based on compact thermal models, such as the Foster and Cauer networks, which can be useful for SPICE-like electro-thermal simulations.
The aim is to show how multiphysics simulations can be used for the cooling system design or for reliability studies.

11:30-12:30 **Best PhD poster award in DCIS 2019.**
Presentation of the contribution in the best PhD poster.
Closing Ceremony. **BAROJA ROOM**

12:30-14:00 Lunch.